Silicon Substrate Integrated Tuneable Ferroelectric Devices for Microwave Applications

S. Gevorgian, A. Vorobiev, D. Kuylenstierna, P. Rundqvist, and S. Abadei

[a)]Department of Microtechnology and Nanoscience, Chalmers University of Technology, 412 96 Gothenburg, Sweden, [b)]Ericsson AB, Mölndal, Sweden
spartak@ep.chalmers.se; spartak.gevorgyan@ericsson.com

I Introduction

Some ferroelectric materials (e.g. $Ba_xSr_{1-x}TiO_3$), especially in paraelectric phase, have low microwave losses $(tan\delta)$ and *DC* field (E) dependent dielectric permittivity, $\varepsilon(E)$, characterised by fractional change (tuneability) $T_\varepsilon(E)=[\varepsilon(0)-\varepsilon(E)]/\varepsilon(0)$. Additionally, they have extremely high permittivity, allowing substantial reduction of the sizes of microwave components since, in most cases, the sizes of these components are proportional to the wavelength of the microwave signals in the dielectric, $\lambda_g=\lambda_o/\varepsilon^{1/2}$, where λ_o is the free space wavelength. Radiation hardness, extremely small leakage currents are the other advantages of these materials making them attractive for wide range of microwave applications, including:

- Varactors and varactor based devices- mixers, harmonic generators, *VCO*s etc;
- Tuneable resonators, filters and antennas;
- Small size tuneable delay lines and phase (time) shifters
- High density capacitors, and small size low impedance transmission lines;
- Thin Film Bulk Acoustic Wave Resonators (*TFBAR*s) and filters
- Surface Acoustic Wave (*SAW*) filters, convolvers, converters et.;
- *MEM* switches (for piezoelectric activation, and/or for increased on state capacitance)

At present, the large-scale applications of ferroelectric components and devices depend on the integration possibilities of microwave ferroelectric components with standard semiconductor processes. In this respect the ferroelectrics are not new in silicon technology. In recent years considerable efforts have been concentrated on the development *CMOS* based memory cells for Dynamic Random (*FERAM*) and nonvolatile memory applications, where ferroelectric capacitors are integrated with *MOS* transistors. Most of the material problems associated with the integration ferroelectrics with standard silicon processes are solved. In addition, there is a considerable progress in developing *CMOS* based *MMIC*s. Thus, there seems to be no major problems in the development of *SiMMIC*s integrating ferroelectric films, where some useful features of ferroelectrics are utilized.

Furthermore, ferroelectrics (i.e. $SrTiO_3$) are considered as a buffer layer to grow *III-V* semiconductors on silicon wafers. Such integration targets several goals, including fabrication of large area (wafer) III-V semiconductors (e.g. *GaN*), and hence merging the advantages of III-V semiconductors with cost effective silicon technologies. Having a ferroelectric (i.e. *STO*, *BSTO*, *PZT*) in *III-V* on silicon structure makes it promising for complex integration of large diversity of optoelectronic, high speed/microwave, and piezoelectric components, sensors etc.

In this report we present recent results on integration of tuneable ferroelectric components with the silicon substrate. The silicon substrates with ferroelectric components are considered for applications in Multichip Modules [1], which is regarded as a step toward the integration of ferroelectric components with silicon MMIC chips.

II Varactors as basic ferroelectric components

Varactors (and non tuneable high density capacitors) may have two basic designs shown in Fig.1. For the parallel-plate design, Fig.1a, the tuneability of the capacitance, $T_c(E)=[C(0)-C(E)]/C(0)$ is practically the same as the tuneability of permittivity, $T_\varepsilon(E)$. The coplanar-plate design, Fig.1b, is simple to fabricate and integrate. However, due to the shunt connected partial capacitances of the substrate (C_{Si}), air (C_{air}), and oxide film (C_{SiO2}), the tuneability of the capacitance is smaller than that of the permittivity $T_\varepsilon(E)$:

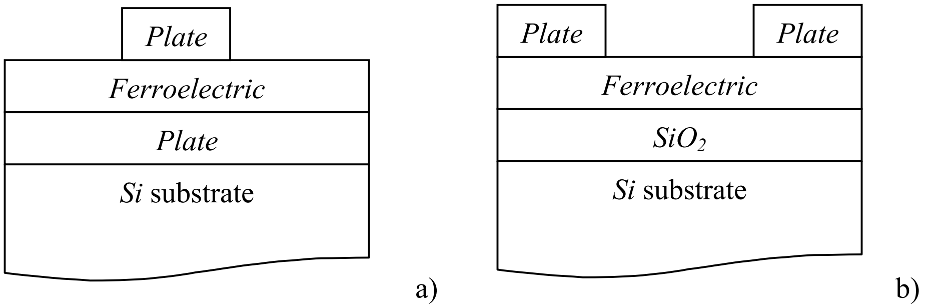


Fig.1 Parallel-plate (a) and coplanar-plate (b) ferroelectric varactors on silicon substrate

$$T_c(E)=[C_f(0)+C_b(0)-C_f(E)-C_b(E)]/[C_f(0)+C_b(E)+C_{Si}+C_{air}+C_{SiO2}] \tag{1}$$

Here $C_b(E)$ is the surface barrier capacitance of silicon. The main problem, in fabrication of both varactors, is to grow epitaxial (quasi-epitaxial) films with low microwave losses and high tuneability.

Table 1 compares the performance of a parallel-plate ferroelectric varactor with the commercially available best semiconductor analogues. The breakthrough performance of ferroelectric varactor shown in Table 1 is achieved by optimised growth of *BSTO* films on a thick gold electrode. The thicknesses of the top and bottom electrodes in this varactor are $Pt(0.1\mu m)/Au(0.5\mu m)$, and the thickness of the *BSTO* film is 0.3 μm. In contrast with the semiconductor analogues, the leakage current of ferroelectric varactor is about three orders of magnitude smaller, and it has symmetric $C(V)$, Fig.2. The losses in our parallel-plate varactor are limited mainly by the losses in the plate, although we expect some reduction of the dielectric losses by further improvement of crystalline structure of the ferroelectric film and film/electrode interface.

Table 1 Comparison of varactors

Company	Model	Material	Quality factor			
			Low frequency	10 GHz	30 GHz	45 GHz
Chalmers	MC-2	BSTO	230@25V(1.0MHz)	100@25V	30@25V	25@25V
			230@0V(1.0MHz)	66@0V	25@0V	22@0V
M/A-Com Inc.	MA 48701E	GaAs	11000@-6V 50 MHz	55@-6V	18@-6V	12@-6V
Metalics Corp.	M SV 34,060 C12	Si	6300@-4V 50 MHz	31.5@-4V	10.5@-4V	7@-4V
M Plus Microwave Inc.	MP 6301	Si	5000@-4V 50 MHz	25@-4V	8.3@-4V	5.5@-4V

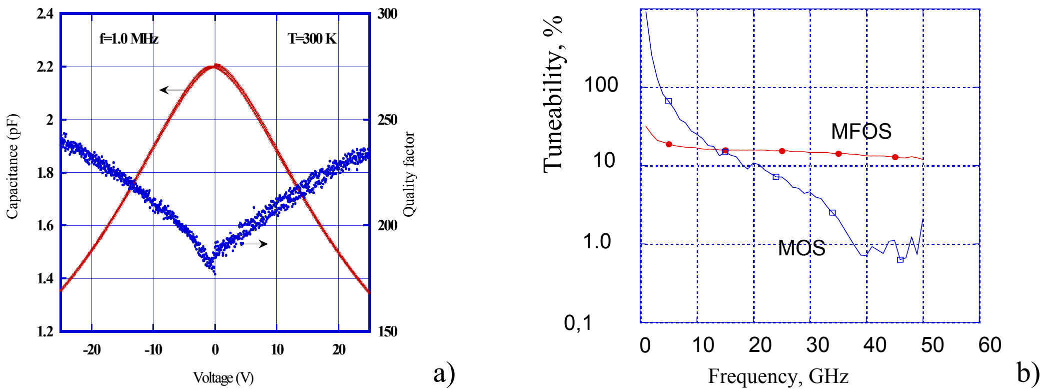


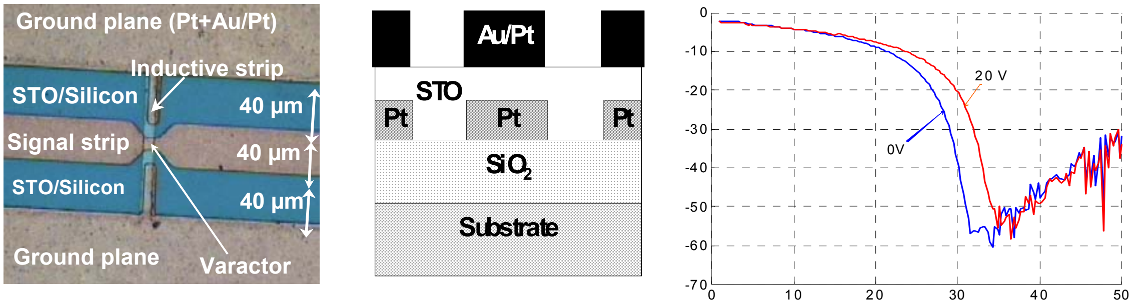
Fig.2 *C(V)* and *Q(V)* of parallel-plate varactor (a), and comparison of coplanar plate ferroelectric varactor *(MFOS)* with standard *MOS* varactor (b)

The *C(V)* performance of the coplanar plate varactor is more complex due to the bias dependent width of depletion layer on the surface of silicon. Fig.2b compares the tuneabilities of standard *MOS* and *MFOS* varactors in a wide frequency range. In the *MFOS* varactor the gold interdigital electrodes are 0.5 µm thick. Each of them has 12.0 µm long five fingers. Slot- and stripwidths are 2.0 µm. The sizes of the contact pads in the horizontal plane are 125x125 μm^2. The tuneability of *MOS* varactor at low frequencies (<10 GHz) is associated with the action of barrier at the silicon surface, i.e. $C_f=0$ in (1). In the *MFOS* varactor the tuneability is associated with both ferroelectric film and surface barrier, as it is indicated in (1). In contrast to the *MOS* varactor, the tuneability at low frequencies is smaller since the electric field is concentrated in the high permittivity ferroelectric film. Only a small portion of the field penetrates in the silicon substrate, and effect of the surface barrier is partly screened by the ferroelectric film ($C_b<C_f$). The barrier capacitance only has some effect below 4-5 GHz.

As it follows from Fig.2b, at higher frequencies, the tuneability of the *MFOS* varactor is due to ferroelectric film only, since the barrier capacitance is not tuneable. The Q-factor of the coplanar-plate varactor depends on the losses in metal plates, ferroelectric film, the resistivity of the semiconductor substrate and the state of the surface barrier (accumulation, depletion, inversion). For microwave application high resistivity (> 2kOhm cm) is preferable for small losses, but it requires good control of surface barrier.

III Device demonstrators

Since the first high Q-factor varactors have been developed several months ago, Table 1, a number of microwave devices have been demonstrated and, more devices are under consideration, including tuneable filters, tuneable delay lines, *VCO*s, and harmonic generators. Fig.3 shows an example of a device based on our ferroelectric varactors fabricated on a high resistivity (>10 kOhm cm) silicon substrate. Shown in Fig.3a is a microphotograph of a fragment from a coplanar waveguide, periodically loaded by parallel-plate ferroelectric varactors. The cross section, Fig.3b, of the varactors in this *CPW* is the same as the parallel plate varactors above: the thickness of the top and bottom electrodes in this varactor are $Pt(0.1\mu m)/Au(0.5\mu m)$, and the thickness of the *BSTO* film is 0.3 μm. This device was designed as a tuneable *1D* electromagnetic (photonic bandgap) crystal. Shown in Fig.3c is the first pass band, where it acts as a low pass filter. Under DC applied field the skirt of this filter shifts (tuning) upwards about 4 GHz (>10%) at –50dB level. By proper design (i.e. as a low pass filter) the skirt of the filter can be made even steeper, and the losses smaller at higher frequencies.



a) *b)* *c)*

Fig.3 Microphotograph (a), cross section (b), and tuneable low pass (S_{21}) filter performance (c) of ferroelectric

IV Conclusions

The state of the art performance ferroelectric varactors integrated with silicon substrate developed at Chalmers open up possibilities and challenges for the development of large variety of microwave devices targeted on industrial applications. The varactors have been characterized at frequencies up to 50 GHz (limited by the measurement set up), however, potentially they are useful up to 100 GHz and above. The tuning speed of the varactors is extremely high. Our recent experiments show that they may be tuned with sub-nanosecond speed. Currently experimental work is underway to study the nonlinear performance and power handling capability.

Partial financial supports from SSF's Oxide and High Speed Electronics programs, CHACH/VINNOVA, and VR are greatly acknowledged.

[1] A concept proposed by Thomas Lewin, Ericsson AB