SoCTRix - A 4G Radio Research Project - Status 2003

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Background and Introduction

SoCTRix is a research demonstrator project, defined and run under the Swedish Socware program. SocTRix serves as a vehicle and focal point for the development of the Socware network, forming a common platform for the active cooperation between partners from national and international industry, universities and research institutes. Acreo is responsible for the management and technical coordination of the project and also takes the responsibility for the system design and development of the actual transceiver hardware and software. This paper briefly describes the scope and some of the achieved results half way into the project.

Project Organization

SoCTRix involves nine industrial partners; Agilent, Samsung, Cadence, VIA Technologies, BitSim, Catena , ARC, Chartered Semiconductor, Jazz Semiconductor, seven universities; LiTH, LTH, KTH, CTH, MDH, Mid Sweden University, and NTNU, and three research institutes; FOI, Shanghai IC R&D and Acreo . SoCTrix is defined to run over 2 plus 1 year, where the third year is optional and targeting the final integration of the design blocks developed during the first two years. The project model allows ideas and results from research at the universities and institutes to be evaluated, implemented, and tested in a ”real” test platform, aiming at a realistic application. A good example of this is the joint design and implementation of the wide-band LNA described in [Andersson]. Industry partners get good insight into and contact with current research as well as actual IP in return for their member fee.

Technical Scope and Goals

SoCTRix is targeting development of technology enabling future 4G applications where there is a need for low cost flexible radio terminals capable of both 3G and Wireless LAN communication. High data throughput or VoIP are supported with local area coverage by WLAN technology in the 2.4 and 5 GHz bands and lower data throughput with wide area coverage are supported through W-CDMA.

In the project, the ultimate goal is to develop a completely integrated radio receiver covering all of these standards and using technologies that are, or will be, available at a competitive cost level within a two to three year time horizon. This will be possible through the common resources and efforts of universities, institutes , and industry but also through the advantage of having control of and access to almost all domains of the design; radio architecture, analogue, mixed signal, and digital circuit design, signal processing and algorithms, and package and substrate design.

Technical Status

At this point in time (Oct-03) the project has run for a little less than half of its projected 24 plus 12 months. The main results, challenges and some of the solutions in the different design domains so far are described in the following sections where special attention is paid to the analogue and radio architecture aspects.

System Design – Technology and physical partitioning

At the outset of the project 0.18µm CMOS was selected as the preferred process. This choice was primarily motivated by the fact that the major part of the system would be digital. The high frequency characteristics of deep submicron CMOS also suggested that it should be a viable alternative for the RF-parts. There are however a number of challenges associated with implementing 5GHz transceivers in CMOS, compared to other technologies such as SiGe BiCMOS. Those are e.g.:

- High 1/f noise, implying reduced performance of VCOs and base band circuits.
- Higher power dissipation for same dynamic range.
- Less mature RF simulation models.
- Low supply voltage, implying reduced dynamic range and transmit output power.

The ambition to keep as much of the system as possible on-chip, as low cost as possible, and provide high flexibility in the analog-digital partitioning, however made CMOS the choice also for the design of the RF parts. For the radio architecture, the requirement on highest achievable level of integration, left only the low- or zero-IF as suitable candidates.. Due to the wide bandwidth of WLAN systems, direct conversion is the architecture of choice, but for W-CDMA both direct conversion and low-IF can be considered. Direct conversion brings about many design issues, e.g. signal dependent DC-offset, quadrature imbalance, VCO pulling, and LO-leakage. These issues are primarily addressed by careful analogue design with respect to isolation, matching, and linearity. To the extent that careful analogue design is not sufficient to achieve the required performance, DSP is utilized for control and correction or residual errors. One example of an algorithm for quadrature error correction developed in the projects is described in [Händel].The resulting direct conversion architecture is outlined in figure 1

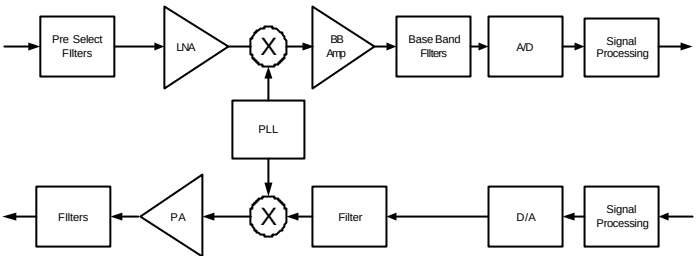

Figure 1 - Radio architecture

At a very early stage in the project there were clear indications that a complete system-on-chip implementation would probably not be technically feasible within the given resource frame. A study was initiated which compared a pure SoC, System-On-Chip, approach with an alternative SoP, System-on-Package , and concluded that the latter has some significant advantages for this application. One of the primary "SoC-killers" is the poor power added efficiency of linear CMOS power amplifiers (PA), which, in combination with the low supply voltage, makes it practically impossible to reach even close to the PA performance required. Others are substrate noise coupling, thermal aspects and design flexibility, which combined make a clear case against a full SoC implementation. SoP on the other hand expands the available design space and offers the system designer to select optimal processes for the very different demands of the power, analogue and digital parts of the radio system. In addition it naturally integrates the package and substrate as a resource for design and can actually result in a denser designs than SoC. Taking these and other aspects into account, it was decided to use a SoP approach with the physical partitioning outlined in figure 2.

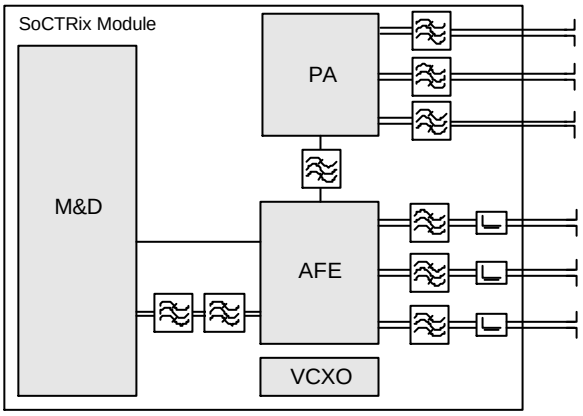

Figure 2 - Physical Partitioning

Antenna design

In order to minimize the number of performance degrading and area consuming switches and baluns an all-out differential architecture has been chosen for the analogue front end. This requires the antenna element(s) not only to support 2.4 and 5GHz transmissions, but also to be balanced. In order to verify that this is possible to achieve, a prototype antenna array consisting of 6 separate elements with a total size of approximately 33cm^2 on ordinary FR4 has been developed and characterized. See fig 3. The results indicate that this is in fact a viable solution and especially that the isolation between the Rx/Tx W-CDMA elements can be made sufficiently high.

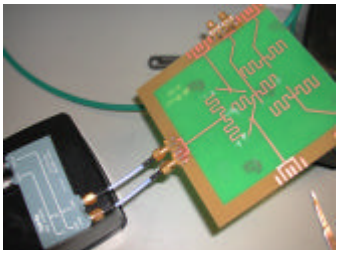

Figure 3 – Antenna under test

Analogue- and RF-IC design

One of the single most challenging tasks of the project is the design of analogue front-end, and especially the RFIC-die, which shall support all of the included standards. In order to achieve sufficient isolation from the noisy digital, mixed and PA-parts, this block is initially implemented in a separate chip, using the same 0.18µm RF-CMOS process as the Mixed/Digital chip. The choice of technology, primarily motivated by processing cost and the SoC-vision, implies a number of specific problems as mentioned above. E.g the supply voltage is limited to 1.8V nom, which means that the design has to be functional down to 1.6V. This severely limits the headroom and dynamic range. Gain, noise level and poor isolation or other issues.

Most of these can however be resolved through workarounds, e.g. deploying an all-out differential architecture, but also by using some of the RF-enhancements offered by the CMOS foundry, like deep-N wells, MIM-capacitors and thicker top-level metal. Up to this date a good part of the RFIC has already been designed. Four tape-outs have commenced and currently a receiver chain for the 802.11 a,b and g standards is being evaluated, see fig 4, and a complete transceiver (FE2) is being taped-out. By the end of April 2004, a complete W-LAN + W-CDMA transceiver is planned for tape-out.

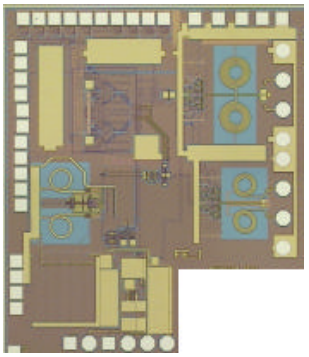

Figure 4 – 802.11abg receiver

PA Design

After thorough studies of process alternatives and topologies, it was decided to develop a differential class-A PA in SiGe (Jazz Semiconductor) suitable for the overall architecture of the demonstrator. Due to power efficiency and matching considerations, a broadband implementation is not considered optimal why the PA will consist of two parallel amplifiers, tuned for 2.4 and 5GHz respectively. To date, a first design of a 24dBm 5GHz PA-core has been designed and taped-out (see fig 5). By April-04 the plan is to tune and complete it with all the functionality required for the demonstrator. Although the task of transforming this design to the 2,4GHz-band is expected to be a fairly straightforward, it will probably not fit into the planned budget and resources of the first two years of the project.

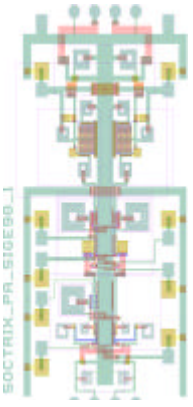

Figure 5 - 5GHz PA

Mixed Signal IC Design

An A/D and D/A converter supporting all of the included standards shall be implemented on the mixed-& digital chip of the demonstrator. The projected requirements for the A/D-converter is 8 to 10 bits of resolution at a sampling frequency of 40MHz. The main challenge is to achieve sufficient linearity and dynamic range at low power dissipation with a supply voltage which is limited by the process to 1.8V. Also, the co-location with the digital parts of the system makes the noise-coupling issues

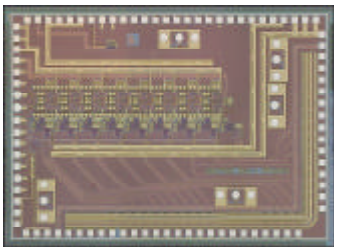

Figure 6 - Mixed signal chip

crucial. This is in part handled through utilizing some of the features of the RF-CMOS process, such as deep-n-well transistors. This far, one 9-stage pipe-lined AD-core has been designed, processed and measured. (See fig 6) The effective number of bits was measured to 8.

Digital IC and Algorithm Design

The digital blocks should ultimately handle both the W-LAN and W-CDMA base-band algorithms required, including transceiver control and error corrections needed for the direct conversion architecture of the analogue front-end. Due to budget and resource limitations, the design in SoCTRix is however restricted to the OFDM modem (802.11a,g). The algorithm development is carried out in Agilent's ADS environment and when sufficient performance is achieved in the system reference simulator the algorithms are implemented in VHDL and prototyped on FPGA. In parallel, Ph.D students are addressing the major challenge to find a architecture that maximizes the reuse of blocks between the different standards. An example of this work is presented in [Tell]. Another challenge, addressed by Ph.D. students, is to find a low complexity digital architecture that enables the use of a single clock for all systems. Even though prototyping is done in FPGA, the ultimate target is ASIC and therefore a first chip (See fig. 7) containing a full implementation of the data-path of an IEEE802.11a base-band transmitter including an FFT [Ullah] has been designed and verified. During the verification process, the measured parameters matched 100% with the simulated values. The final implementation of the digital block is estimated to require some 2 million Gates (NAND equivalents) and consume a chip-area of 20mm^2.

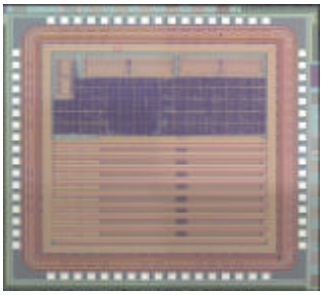

Figure 7 - First digital chip

Outlook

By April-04, most blocks required for a transceiver module supporting 802.11abg and W-CDMA will be ready. The third year was originally planned for integration of these blocks into the final demonstrator. At this point however, the financing still remains to be settled. For the interested, the progress of the project can be monitored via the regular reports published on EE times.

Summary

An overview and current status report of the SoCware demonstrator project SoCTrix has been given. Some of the major technical challenges, trade-offs and decisions have been described, with special attention given to the problems related to implementing GHz-circuits on CMOS. Finally an outlook of the remaining activities of the project was presented.

References

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