50-nm GATE-LENGTH InP-BASED HEMTs FOR MILLIMETER-WAVE APPLICATIONS

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SUMMARY

InP-based HEMT technology presents substantial performance advantages for millimeter wave applications such as high-speed wireless communications, radio astronomy, and radar. We report on the development of a 50-nm gate-length process for millimeter wave InP HEMTs. The gate patterns were defined using a single electron beam exposure and a bi-layer resist system. The process was evaluated on pseudomorphic InAlAs/InGaAs/InP HEMT material. A two-finger, 100 μm gate-width device showed an extrinsic DC peak transconductance of 650 mS/mm at V_{ds} = 1.0 V. At the same drain bias, the transit frequency and the maximum frequency of oscillation were 180 and 230 GHz respectively. The developed 50-nm process constitutes the new baseline for the InP MMIC process at the Microwave Electronics Laboratory at Chalmers.

INTRODUCTION

InP-based InAlAs/InGaAs high-electron mobility transistors are the most promising devices for millimeter- and sub millimeter wave applications. Due to the high electron mobility and carrier velocity combined with large electron sheet densities, cut-off frequencies approaching 600 GHz are realizable [1-3]. This development has made it possible to design and manufacture monolithic millimeter wave circuits that operate above 200 GHz [4-6]. Key factors to achieve this performance are the design and growth of high-quality pseudomorphic epi-material, gate-lengths below 100 nm, and the avoidance of short-channel effects. In this study, we developed 50-nm gate pseudomorphic HEMTs with reduced gate-to-channel distance, based on previously developed concepts and procedures. The 50-nm HEMT has been implemented in a demonstrator wideband amplifier circuit.

MATERIAL DESIGN

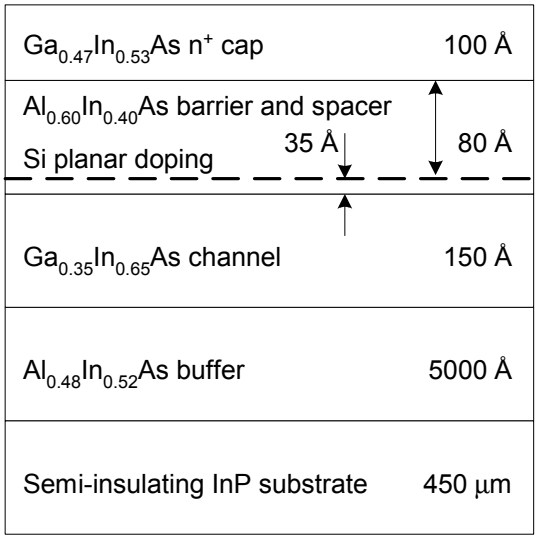

Figure 1
Epitaxial structure of the InP HEMT.

The layers of the HEMT were grown by MBE on a Fe doped semi-insulating InP substrate. The epitaxial structure consisted of an InAlAs buffer, a strained InGaAs channel, a strained InAlAs spacer layer, a Si doping plane, a strained InAlAs Schottky layer, and an n^+ InGaAs cap layer. The various layer thicknesses and compositions can be found in Figure 1. The thin barrier and spacer layer of 115 Å is necessary to keep a short gate-to-channel distance, thereby suppressing short-channel effects [7]. Hall measurements revealed a two-dimensional electron gas (2DEG) sheet density of 2.72×10^{12} cm^{-2} and a room temperature mobility of 10,100 $cm^2V^{-1}s^{-1}$.

DEVICE FABRICATION

The devices were fabricated by a combination of optical and electron beam lithography (EBL) techniques. Mesa isolation was achieved by a phosphorus acid-based wet chemical etch. The channel edge was slightly etched using a selective citric acid and hydrogen peroxide mixture. This recess etch prevents the gate metal to contact the channel at the mesa wall. A potential gate leakage current was reduced in this way. Source and drain ohmic contacts with 2 μm spacing were defined by a lift-off procedure and subsequently annealed. The resulting contact resistance was 0.2 Ωmm.

The mushroom-shaped gates were defined in a two-layer resist system consisting of PMMA and Copolymer. A single exposure was performed in a 100 kV JEOL JBX9300FS electron beam lithography system under conditions that nominally result in a 5-nm diameter beam. A low dose exposure defined the width of the gate head and a high dose defined the footprint. The two resist layers were then developed using different developers, ECA (2-etoxietylacetate) for the Copolymer and toluene for the PMMA. To achieve the desired gate geometry both exposure doses and developing times were varied and the result was evaluated using a scanning electron microscope (SEM). The gate recess etch was performed using a selective citric acid hydrogen peroxide solution at a controlled temperature. Titanium, platinum, and gold were evaporated to form the gate electrodes. Figure 2 shows a SEM micrograph of the gate cross-section.

The devices were passivated by a 700 Å thick reactively sputtered silicon nitride layer. Openings for transistor pads were formed by optical lithography and a dry etch (RIE) using NF_3. In the final fabrication step gold was grown by electro plating on the transistor pads and air-bridges for source interconnections were formed. Figure 3 shows a SEM micrograph of an air-bridged device with four gate fingers.

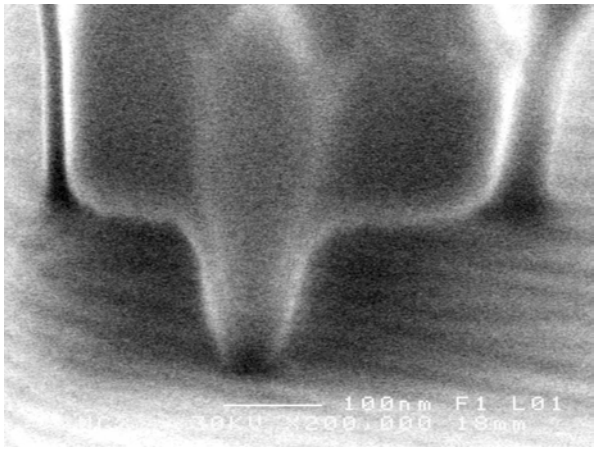

Figure 2
SEM micrograph of the 50-nm gate cross-section.

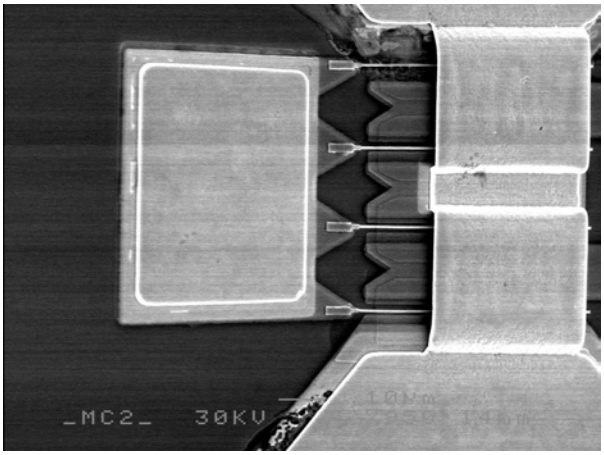

Figure 3
SEM micrograph of an air-bridged, four gate-finger device.

DEVICE PERFORMANCE

The DC current-voltage (I-V) characteristics of unpassivated 2x50 μm devices were measured on-wafer using a semiconductor parameter analyzer and are found in Figures 4-5. The devices show good pinch-off characteristics and an extrinsic peak transconductance of 650 mS/mm at a drain-source voltage of 1.0 V.

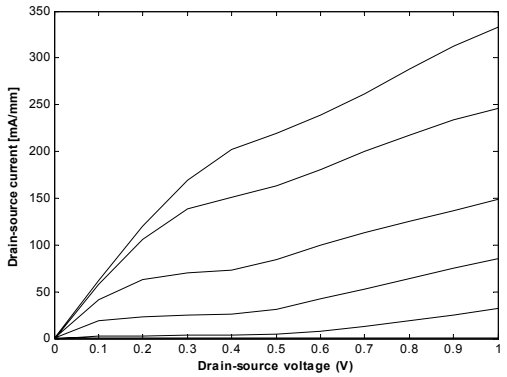

Figure 4
Current-voltage (I-V) characteristics of a 50-nm HEMT with 2x50 um gate-width. The gate-source voltages are from bottom to top: -0.7 (coincides with X-axis), -0.35, -0.25, -0.15, 0.0, and 0.175 V.

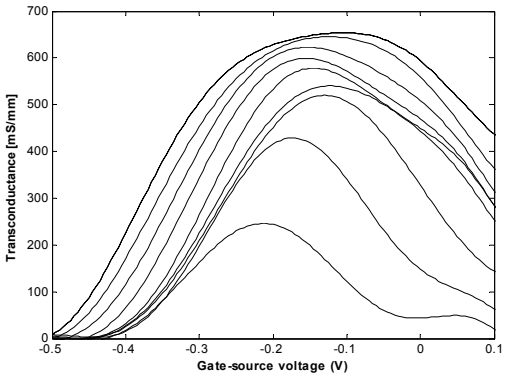

Figure 5
DC transconductance (gm) characteristics a 50-nm HEMT with 2x50 um gate-width. The drain-source voltage Vds was varied from 0.1 V (bottom) to 1.0 V (top) in 0.1 V steps.

The S-parameters were measured on-wafer to 50 GHz using a probe station and vector network analyzer. Current gain ($|h_{21}|^2$) and unilateral power gain (U) versus frequency were extracted from the data, see Figure 6.

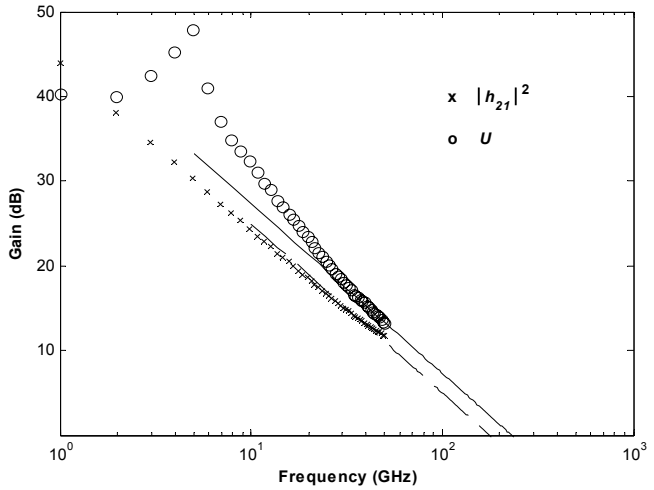

Figure 6
Extracted current gain $|h_{21}|^2$ and unilateral power gain U for a 2x50 µm HEMT. The source-drain voltage V_{ds} was 1.0 V and the gate-source voltage V_{gs} was –0.2 V. An f_T of 180 GHz and an f_{max} of 230 GHz was estimated from extrapolating the curves with a slope of –20 dB/decade.

To demonstrate the integration of the 50-nm devices into a monolithic integrated circuit process, a broadband, single-stage, resistive feedback amplifier was designed and manufactured (Figure 7). The amplifier was designed around a 2x50 um device and had a 10-ohm resistor and a 1.2-pF capacitor in the feedback loop. To improve stability, the drain was loaded with a 10-ohm resistor in series.

The fabrication process followed the HEMT fabrication, with the following additions. Prior to the gate definition, the resistors were fabricated in thin film technology using reactively sputtered tantalum nitride (TaN) and a lift-off procedure. The bottom plate of the capacitor was deposited directly on the semi-insulating InP substrate and the top plate on the dielectric right after device passivation. To improve the reliability of the capacitor, the thickness of the passivation layer was increased to 2000 Å, which resulted in a nominal capacitance of 300 pF/mm^2. The capacitor top plate was connected to the transmission line using an electroplated air bridge. In the same step, gold was grown on the transmission lines and pads. The chip was thinned down to 75 µm and via holes were etched from the backside. Finally, a 3-µm thick backside metal layer of gold was electroplated. The S-parameters of the amplifier were measured on-wafer using coplanar probes with a network analyzer. The amplifier exhibited more than 8-dB gain over a 0-42 GHz band at a DC power of 27 mW.

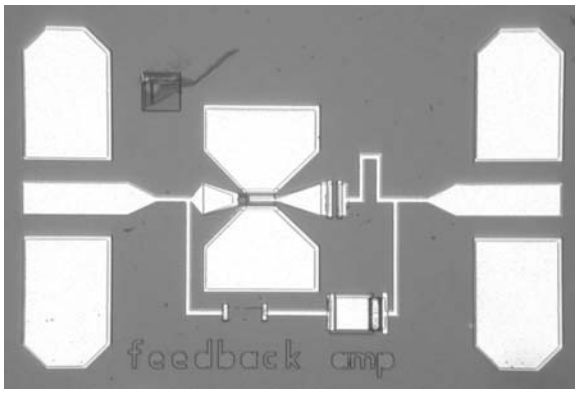

Figure 7
Photograph of the feedback amplifier.

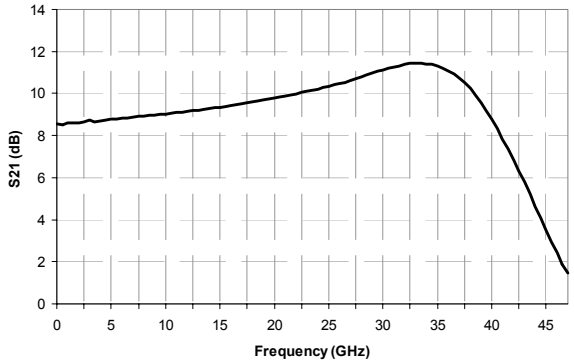

Figure 8
Measured S_{21} for the feedback amplifier.

CONCLUSION

We have fabricated and characterized a new generation of millimeter wave InP HEMTs employing 50 nm gates. The device technology was demonstrated through a broadband, single-stage, resistive feedback amplifier that exhibited more than 8-dB gain from zero to 42 GHz.

ACKNOLEDGEMENT

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