# Noise Parameter Modeling of HEMTs and Nanometer-Scale CMOS Transistors with Gate Leakage Currents

Hans-Olof Vickes and Mattias Ferndahl[+]

Ericsson Microwave Systems AB, SE-431 84 Mölndal, Sweden.

[+]Chalmers University of Technology, Microwave Electronics Lab., SE-412 96 Göteborg, Sweden

*Abstract* — **Closed-form expressions for the gate-leakage resistance, Rp and its associated noise temperature, Tp, are presented. Tp represents the noise contribution caused by the gate-current Ig. Both Rp and Tp are expressed as functions of the measured noise parameters Rn, Fmin and Zopt. We present both frequency independent expressions and frequency dependent equations and discuss their accuracy. Unique relationships between the measured noise parameters are discussed in addition to the effect on measurement accuracy, careful de-embedding and physical relevance of the model used. Based on this extended three-temperature noise model [1], we show by measurements on HEMTs and 90 nm CMOS transistors, that we can model Rn, Fmin and Zopt very accurately at least up to 26 GHz. In addition, the CMOS model has been verified by S-parameters up to 62.5 GHz.**

## I. INTRODUCTION

Gate-leakage has been reported earlier, eg. [1]-[3], and it has been demonstrated that gate-leakage affects the noise performance, especially at low frequencies. Reuter et al. proposed [1] an extended three temperature noise model which is built on the established description by Pospieszalski [4]. Ikalainen [2] use the two temperature model as shown in [4] but with the inclusion of a resistor to model the leakage of the Schottky gate. Pritchett et al. [3] use S-parameters to extract this resistor. In addition they use Johnson sources at input and output ports to model the overall noise contribution. In this paper we use the model proposed by Reuter et al. [1] and show how these new parameters can be determined from the measured noise parameters.

In this work, we show for the first time, that the three temperature model works for both HEMTs and nanometer-scale CMOS transistors.

To better understand this gate-leakage modeling we present new expressions of how we can determine the new parameters from the measured noise parameters.

## II. NOISE MODEL OF HEMT

A physically relevant model of a transistor can be described with the equivalent circuit shown in Fig. 1. The intrinsic part of the device is detailed in Fig.2.

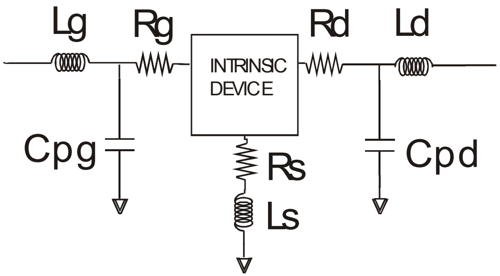

Fig. 1. Small-signal equivalent circuit of the HEMT

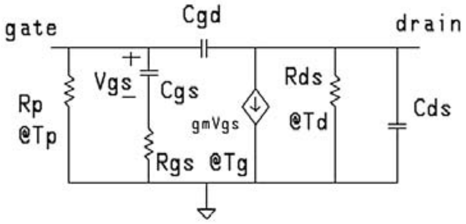

Fig. 2 Extended equivalent intrinsic part of the transistor with three temperatures.

## III. NOISE PARAMETERS AT LOW FREQUENCIES

The derivation of the equations can be done in several ways, but in this paper we used the method described in [5]. By solving a second order equation for low frequency we get

$$\frac{R_P}{T_P} = \frac{(R_{OPT}^L)^2}{T_0 R_n} \qquad (1)$$

where we assumed $(R_P)^2 >> (R_{OPT})^2$

By using the definition of $F_{\min}$ we can simply express $R_p$ and $T_p$ in terms of the low frequency measured noise parameters,

$$R_P = \frac{2 R_n^L R_{OPT}^L}{R_{OPT}^L (F_{\min}^L - 1) - 2 R_n^L} \qquad (2)$$

$$T_P = \frac{2T_0 (R_n^L)^2}{R_{OPT}(R_{OPT}^L(F_{\min}^L - 1) - 2R_n^L)} \tag{3}$$

Knowing these values, we can express the low frequency limits of the noise parameters;

$$F_{\min}^L = 1 + 2R_n^L\left(\frac{1}{R_{OPT}^L} + \frac{1}{R_P}\right) \approx 1 + 2\frac{R_n^L}{R_{OPT}^L} \tag{4}$$

$$R_{OPT}^L = \sqrt{\frac{R_P R_n^L T_0}{T_P}} \tag{5}$$

$$X_{OPT}^L = \frac{\omega C_{gs}}{a \cdot g_m^2}\,;\, a = \frac{T_P R_{ds}}{R_P T_d} \tag{6),(7}$$

$$R_n^L = \frac{1}{T_0}\left(T_g R_{gs} + \frac{T_d}{R_{ds} g_m^2}\right) \tag{8}$$

Measurement of the noise parameters of an active device is difficult at low frequencies. The on-wafer measurements using the ATN NP5B have a low frequency limit at 2.0 GHz. To avoid improper extrapolation down to low frequency, a more practical approach is to use frequency dependent equations. In section IV we will further examine this possibility.

However, what we achieved up to now is the central quotient (1) and the interesting denominator in (2) and (3). The inequality

$$R_{OPT}^L(F_{\min}^L - 1) > 2R_n^L \tag{9}$$

must be fulfilled. This inequality is consistent with that of Pospieszalski [4]. He states that if a model claims to have a physical relevance it must satisfy

$$1 \le \frac{4\,NT_0}{T_{\min}} < 2 \tag{10}$$

Our low frequency inequality satisfy the upper bound of equation (10).

## IV. FREQUENCY DEPENDENT NOISE PARAMETERS

Including frequency now in the calculations, we get the expressions

$$F_{\min}^L(f) = 1 + 2R_n(f)\left(\frac{1}{R_P} + \frac{R_{OPT}^L(f)}{\left|Z_{OPT}^L(f)\right|^2}\right) + \frac{2T_d R_{gs}}{R_{ds} T_0}\left(\frac{f}{f_T}\right)^2$$

(11)

$$R_{OPT}^L(f) = \frac{R_{OPT}^i}{1 + a\left(\frac{f_T}{f}\right)^2} \cdot \sqrt{1 + a\left(\frac{f_T}{f}\right)^2 \cdot \left|\frac{Z_{OPT}^i}{R_{OPT}^i}\right|^2} \tag{12}$$

$$X_{OPT}^L(f) = \frac{X_{OPT}^i}{1 + a\left(\frac{f_T}{f}\right)^2} \tag{13}$$

where

$$R_n(f) = \frac{T_g}{T_0} R_{gs} + \frac{T_d}{T_0 R_{ds} g_m^2} + \frac{T_d R_{gs}^2}{T_0 R_{ds}}\left(\frac{f}{f_T}\right)^2$$

(14)

$$R_{OPT}^i(f) = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{R_{gs} T_g R_{ds}}{T_d} + R_{gs}^2} \tag{15}$$

$$X_{OPT}^i(f) = \frac{1}{\omega C_{gs}} \;(16);\quad f_T = \frac{g_m}{2\pi C_{gs}} \tag{17}$$

and

$$Z_{OPT}(f) = R_{OPT} + jX_{OPT} \tag{18}$$

To overcome the difficulties mentioned in section III, we now have the frequency dependent expressions

$$R_P(f) = \frac{2R_n(f)\frac{\left|Z_{OPT}^L\right|^2}{R_{OPT}^L}}{\frac{\left|Z_{OPT}^L\right|^2}{R_{OPT}^L}\left(F_{\min}^L(f) - 1 - \frac{2T_d R_{gs}}{R_{ds} T_0}\left(\frac{f}{f_T}\right)^2\right) - 2R_n(f)}$$

(19)

$$\frac{R_P}{T_P} = \left(\frac{f_T}{f}\right)^2 \frac{R_{ds}}{T_d} \frac{\mathrm{Im}(Z_{OPT}^L)}{\mathrm{Im}(Z_{OPT}^i - Z_{OPT}^L)} \quad (20)$$

(19)-(20) are robust and give us the desired values if a careful de-embedding is done [6].

## V. MEASUREMENTS

To verify this simple gate-leakage modeling, measurements have been done on MMIC transistors from OMMIC. These are transistors from their commercially available process ED02AH. In this paper we show results from the measurements on a device with 8 gate fingers, each 50 µm wide yielding a total gate width of 400 µm. The excitation is Vds=3.0 V and Ids= 50 mA. Measurements are performed in the frequency range 2.0 – 23.0 GHz.

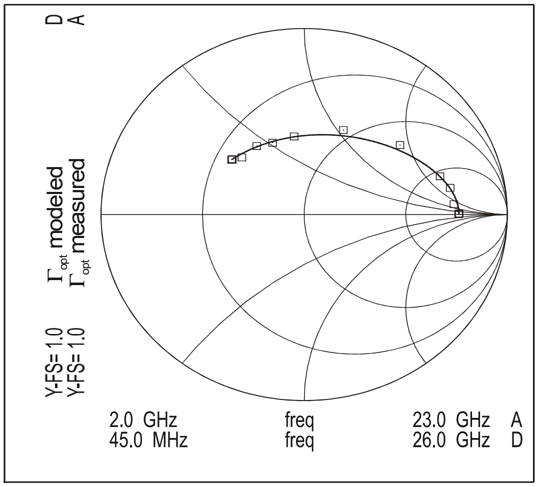

Fig. 3. Comparison of measured Zopt ( ) and modeled Zopt ( — )

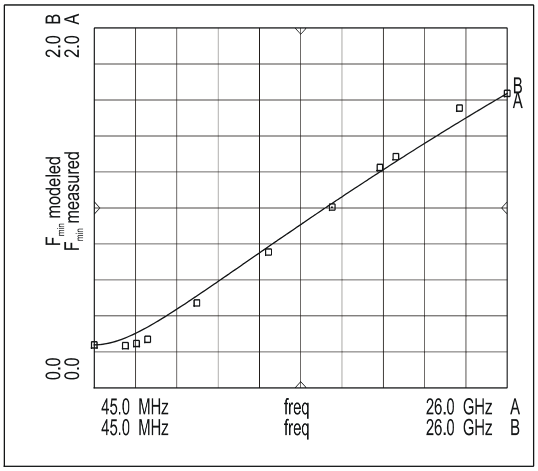

Fig. 4. Comparison of measured Fmin ( ) and modeled Fmin ( — ).

Elements of the small-signal equivalent circuit of the OMMIC transistor biased at Vds=3.0 V and Ids=50 mA are; Parasitic elements: Lg =Ld= 42.2 pH, Ls = 12.8 pH, Rg=1.9 Ω, Rd = Rs = 1.2 Ω, Cpg = 48 fF, Cpd = 40.8 fF.

Intrinsic elements: Rp = 50 kΩ, Rgs = 4.7 Ω, Rds = 56.0 Ω, gm = 211 mS, Cgs = 0.303 pF, Cgd = 0.060 pF, Cds = 0.080 pF, tau = 1.3 ps, Tp = 1096 K, Tg = 310 K, Td = 1355 K.

Without any de-embedding procedure the quotient (1) can be estimated. For the excitation, Vds =3 V and Ids =50 mA, the ratio Rp to Tp was estimated to be in the range 42-49. The uncertainty is mainly governed by the low frequency extrapolated value of Ropt. In the final tuning of the device we achieved the ratio 46.2.

## VI. NOISE MODEL OF CMOS

The same approach used for the HEMT transistor to model the gate leakage current have also been implemented in a CMOS transistor model, see Figure 5.

The device are made in a 90 nm gate length CMOS technology from IMEC, Belgium, with 5 metal layers of damascene Cu and 1.5 nm thick gate oxide. The silicon substrate resistivity is 20 Ωcm.

The total gate width of the CMOS transistor under investigation is 40 µm, 20 fingers with 2 µm width each.

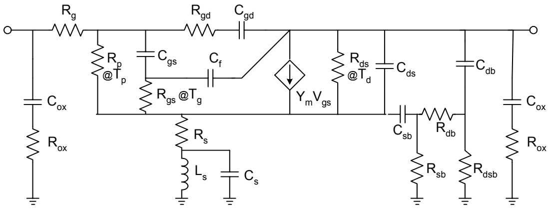

Fig. 5 Equivalent intrinsic part of CMOS model with three temperatures.

## VII. MEASUREMENTS OF CMOS TRANSISTOR

The 90 nm CMOS transistor have been measured up to 62.5 GHz for the S-parameters and up to 26 GHz for the noise parameters. Bias conditions; $V_{gs}$ = 0.8 V, $V_{ds}$ = 1.5 V, $I_d$ = 14.2 mA. This bias condition corresponds to maximum transconductance, $g_{m,max}$ .

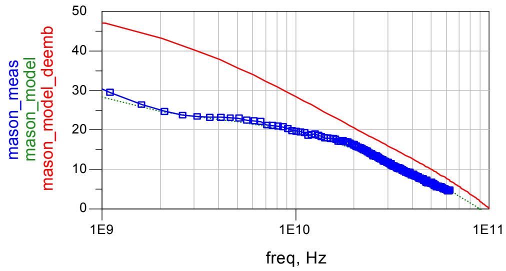

Fig. 6 Mason's gain[dB]. Measured (Blue □) and model (Green dots). De-embedded performance in solid red.

From Figure 6 it is observed that the high frequency performance is excellent. Mason's gain, usually denoted U, can be expressed in the two-port admittance parameters;

$$U = \frac{|y_{21} - y_{12}|^2}{4(g_{11}g_{22} - g_{12}g_{21})} \qquad (21)$$

where $g_{ij} = \mathrm{Re}\{y_{ij}\}$. We get the figure of merit $f_{max}$, maximum frequency of oscillation, when U=1. For our device $f_{max}$ = 90 GHz embedded and $f_{max}$ = 100 GHz de-embedded.

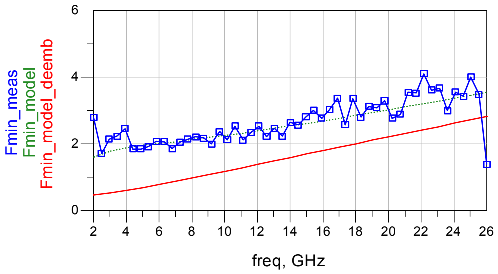

Fig. 7 $F_{min}$ [dB]. Measured (Blue □) and model (Green dots). De-embedded performance in solid red.

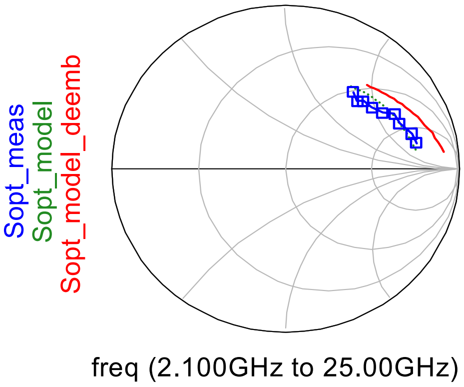

Fig. 8 Optimum impedance, $Z_{opt}$. Measured (Blue □) and model (Green dots). De-embedded performance in solid red

The measured and modeled frequency response of $F_{min}$ are shown in Figure 7. We observe a very good match between the embedded measured and modeled characteristics. We also show the de-embedded frequency response of the model. It is basically 1 dB lower over the frequency interval in comparison with the embedded response.

## VIII. CONCLUSION

A simple modeling of gate-leakage has been presented and implemented for both GaAS HEMTs and Si CMOS transistors. By deriving a new set of equations we could accurately determine the new parameters. We discussed difficulties in the extraction of the parameters at low frequencies and suggested frequency dependent expressions that solved the sensitivity problem at low frequency. In particular, the new expressions are helpful in both the optimization process and the de-embedding procedure and introduce new relationships between the measured noise parameters.

## ACKNOWLEDGEMENT

Part of this work has been supported within the IMPACT-project, IST- 2000-30016. The first author wish to acknowledge the support of The Antenna & Microwave Technology Department, FX/B, at Ericsson Microwave Systems AB, Mölndal, Sweden.

## REFERENCES

[1] R. Reuter, S. Waasen, F. J. Tegude, "A New Noise Model of HFET with Special Emphasis on Gate-Leakage", *IEEE Electron Device Letters*, Vol. 16, No. 2, pp. 74-76, Feb. 1995.

[2] P. K. Ikalainen, "Extraction of Device Noise Sources from Measured Data Using Circuit Simulator Software", *IEEE Trans. Microwave Theory and Tech.*, Vol. 41, No. 2, Feb. 1993.

[3] S. Pritchett, A. Fernandez, D. Bridges and K. Whelan, "Improved FET Noise Model Extraction Method for Statistical Model Development", *1995 MTT-S Int. Microwave Symp. Dig.*, Vol. 2, pp. 943-946, June 1995.

[4] M. Pospieszalski, "Modeling of Noise Parameters of MESFET´s and MODFET´s and their Frequency and Temperature Dependence", *IEEE Trans. Microwave Theory and Tech.*, Vol. 37, pp. 1340-1350, Sept. 1989.

[5] M. Garcia, J. Stenarson, H. Zirath, I. Angelov, "An Algebraic Method for Noise Parameter Analysis of Temperature Noise Models", *Microwave and Optical Technological Letters,* Vol. 17, no. 5, pp. 287-291, 1998.

[6] H. Hillbrand and P. Russer, "An efficient method for computer-aided noise analysis of linear amplifier networks," *IEEE Trans. Circuits Syst.,* vol. CAS-23, pp.235-238,Apr.1976.