FDTD analysis of multichip vertical interconnects

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Abstract

In this paper we present FDTD simulations for multichip interconnects between a CPW transmission line, CPW transmission line and a CPW chip (CPW-CPW-CPW) using metallic, spherical bumps. We show that the main influence on the performance of the entire CPW-CPW-CPW structure has the first level of interconnection, where the via holes are used. A reduction in return loss can be achieved by using small bump dimensions in the lower CPW-CPW interconnection.

Introduction

A standard wire bonding connection has high inductance due to the length of the bonding wire. This inductance is a severe limitation for high quality, high frequency applications. Flip chip interconnections have several advantages over the wire bonding interconnections. The main advantage is the bump's inductance. It can be less than 10% of a bonding wire. Metallic bumps provide also heat sinks due to a lower thermal resistance than semiconductor substrates. This improves the chip power handling capability. Thus the flip chip is highly interesting as an emerging technology for high frequency applications [7]. Flip-chip technology allows several chips to be mounted together on the same motherboard. This increases density, improves system performance and reliability and reduces the cost. The connections between the motherboard and the chip are obtained by applying conductive adhesives or metallic bumps. The geometry and design of the connection pads and bumps are very important for the performance of the connection. Very often we have a few types of the bumps shape, depending on the technology used in the flip-chip mounting. In this case we use metallic, spherical bumps with height and pad diameter equal to 0.8 of the middle diameter of the bump.

Multichip connection

Fig. 1 shows a CPW-CPW-CPW flip-chip bonded circuit. The lines on the both motherboards and on the chip are designed as 50Ω coplanar waveguides (CPW). For the CPW transmission lines the LTCC substrate thickness is 200μm and for the CPW chip the SiGe substrate thickness is 200μm. Top view of the multichip transition is shown in Fig. 1. Connection between Motherboard-1 and lower surface of the Motherboard-2 is achieved by Bumps-1. We start with 400μm diameter in the middle of the bumps. To connect the lower surface of the Motherboard-2 with the upper surface of the Motherboard-2 we need six via holes in the Motherboard-2, as shown in Fig. 1c. Connection between the upper surface of the Motherboard-2 and the chip is achieved by Bumps-2 with 125μm in diameter. We start the analysis with large dimensions of the Bumps-1, and we show that they have large influence on the performance of the transition, especially at higher frequencies. A change in the dimensions of the Bumps-1, results also in a change of the diameter of the Bumps-1 pads. This connection can be described by an inductance and a capacitance. The inductance is due to the bump pad diameter and also due to the bump height. The capacitance is due to the dielectric loading by the chip and is determined by the bump pad diameter. In practice, for typical bump dimensions, the capacitance has larger influence on the performance of the transition than the inductance [4].

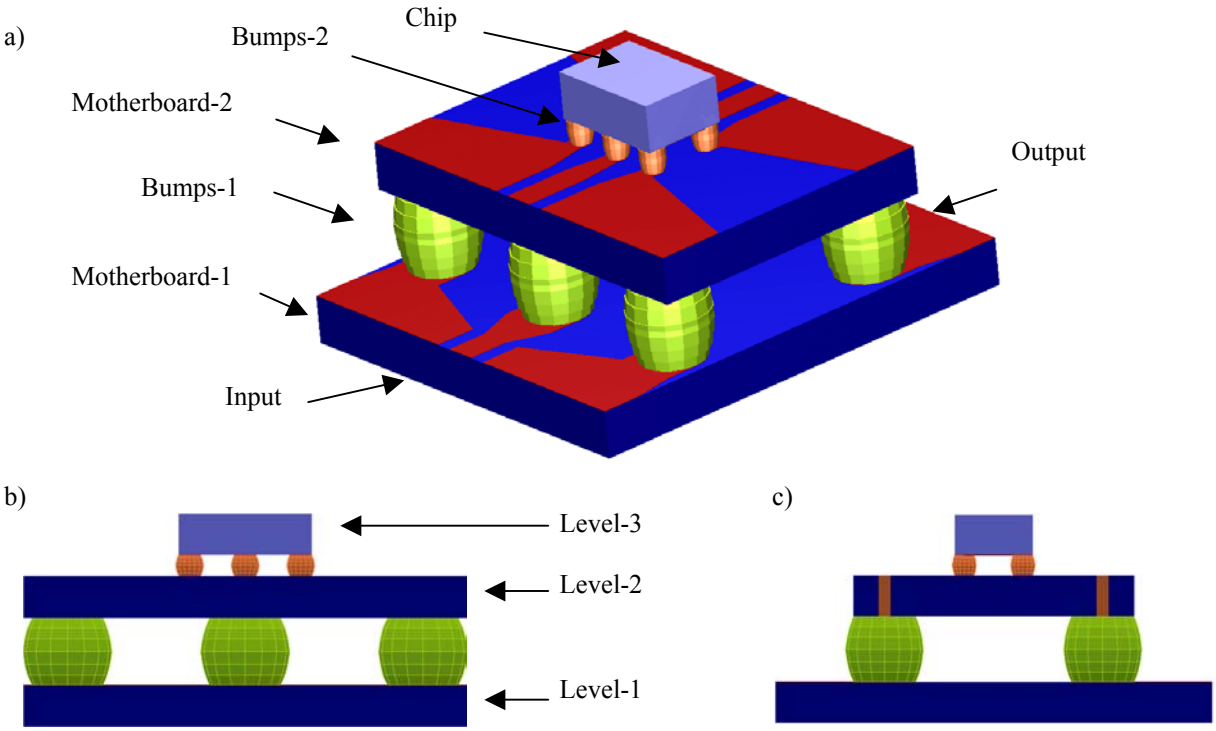

Fig. 1. Multichip structure: a) entire structure, perspective view, b) front view, c) side view

The entire structure is large and it is difficult to optimise it as a one unit. We divide the entire structure into two parts: a lower one, Level-12, and an upper one, Level-23. We analyze the parts separately as follows:

1. Level-12 – input and output is on the Motherboard-1; the upper part is removed
2. Level-23 – input and output is on the Motherboard-2; the lower part including the via holes is removed.

For each of these two structures we try to find optimal dimensions and shape to obtain good performance of the transitions. Next we run the analysis of the entire structure.

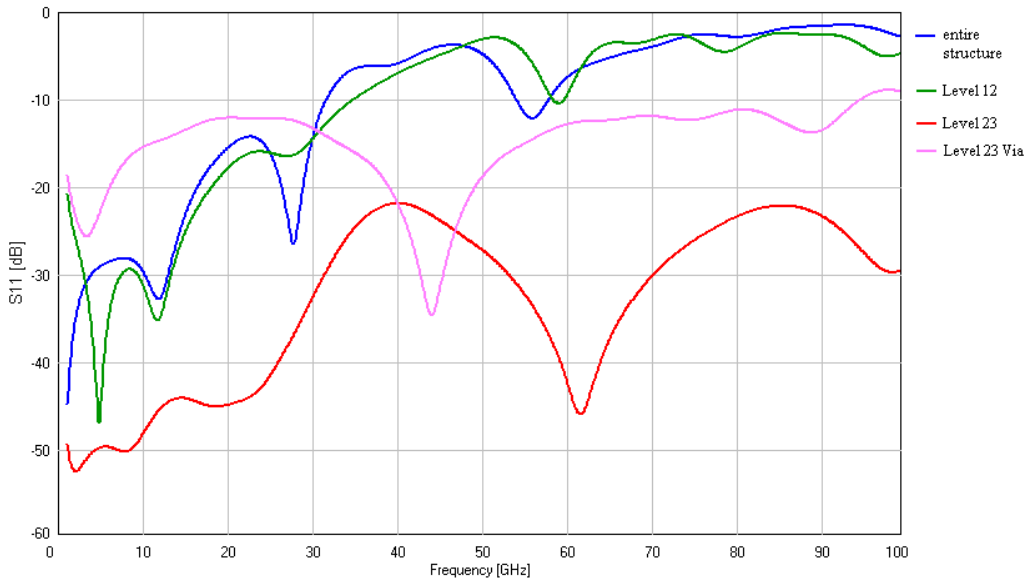

Fig. 2. Simulated s_{11} for entire structure, structure Level-12, structure Level-23 without via holes and for structure Level-23 with via holes.

All simulations were performed with the QuickWave 3D FDTD Simulator [1]. As we can see in Fig. 2 the main influence on the performance of the structure has the connection between Level-1 and Level-2, where we have comparable simulated results as for the entire structure, green and blue curve in Fig. 2. The performance of the upper structure with connection between Level-2 and Level-3 without the via holes to the lower part of Level-2 is very good, red curve in Fig. 2. With the addition of the via holes we can see a considerable deterioration of the return loss, magenta curve in Fig. 2. We attempt to optimise the Level-23 structure including the via holes. For the optimisation the input port is on the lower surface of the Motherboard-2. The connection consists of the via holes to the upper surface of the Motherboard-2, CPW lines on the upper surface of Motherboard-2, via holes to the chip and back the same way to the lower surface of the Motherboard-2. We have simulated three different configurations of Level-23, Fig. 3. In Fig. 3a –b the Bumps-1 pitch is 0.56 mm, in Fig. 3c the pitch is 0.4 mm.

a) b) c)

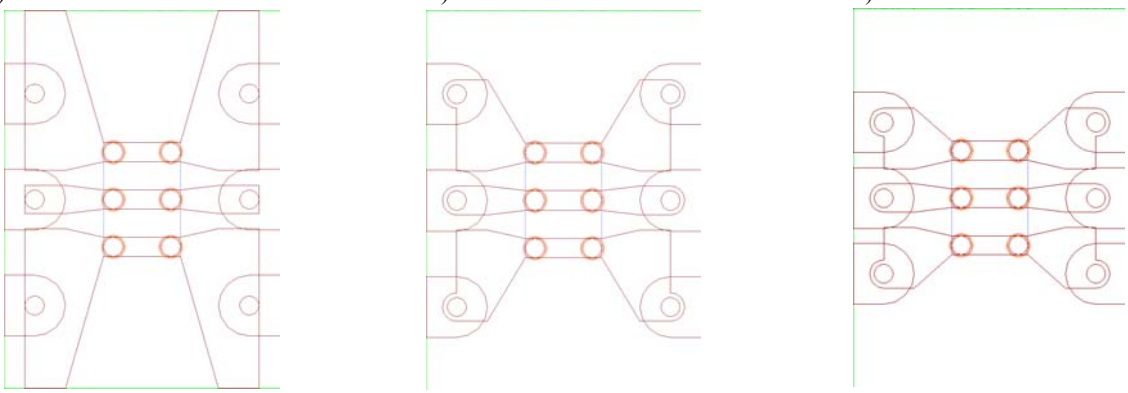

Fig. 3. Level-23 with via holes before and after optimisation: a) original configuration, b) optimised configuration with 0.125mm via hole pad, c) same as b) with 0.4mm Bumps-1 pitch. Bumps-1 diameter is 0.4mm for all cases.

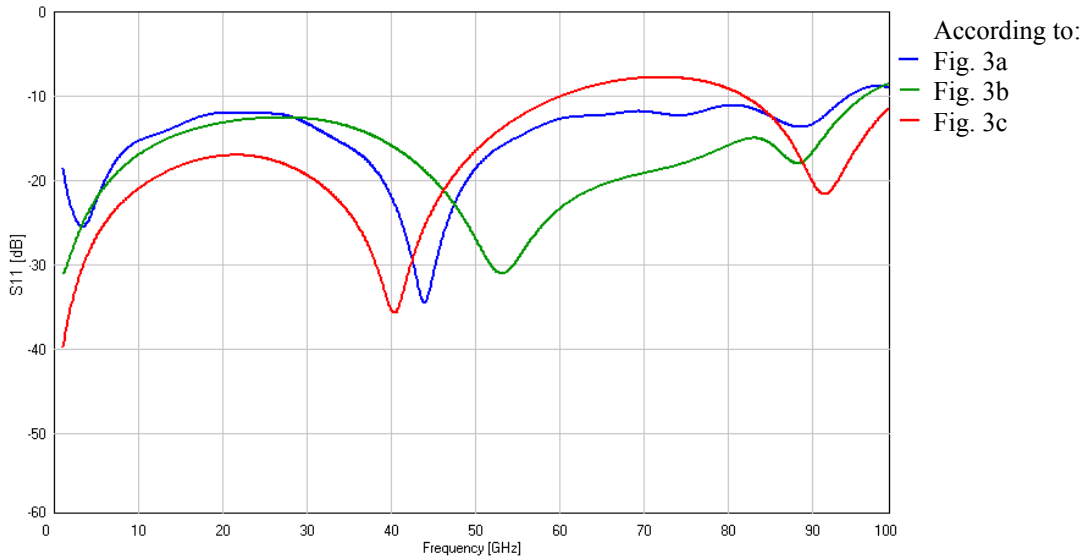

Fig. 4. Simulated s_{11} for Level-23 with via holes before and after optimisation.

Fig. 4 shows the simulated results for structures shown in Fig. 3. For the structure with 0.125mm via hole pad and 0.56mm Bumps-1 pitch, as shown in Fig. 3b, the simulated results are better for higher frequencies, than for the structure with 0.125mm via hole pad and 0.4mm Bumps-1 pitch, as shown in Fig. 3c.

We assemble all levels again and optimise the entire structure for different dimensions of Bumps-1 and different pitches at this level. Fig. 5 shows the simulated structures. As we can see in Fig. 6, the best simulation results are obtained for small diameter of the Bumps-1, 0.125mm. This implies that the Bumps-1 pad diameter is also small (0.8x0.125mm=0.1 mm).

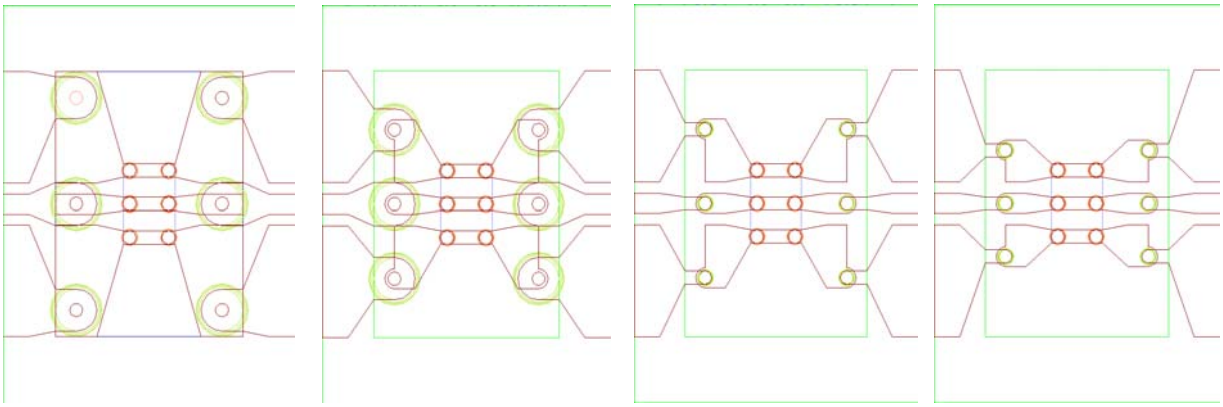

Fig. 5. Entire structures before and after optimisation: a) original structure, b) optimised configuration with 0.56mm Bumps-1 pitch, c) same as b) with 0.125mm Bumps-1 diameter, d) same as c) with 0.4mm Bumps-1 pitch

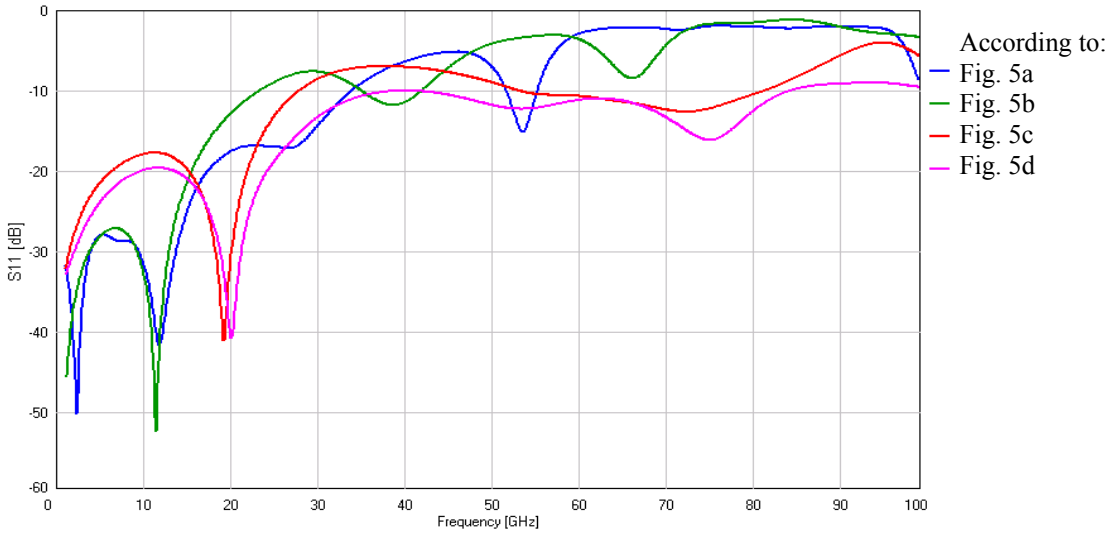

Fig. 6. Simulated S11 for entire structure as shown in Fig. 5.

Conclusions

Multichip interconnects between a CPW transmission line, CPW transmission line and a CPW chip (CPW-CPW-CPW) using metallic, spherical bumps have been investigated. Optimized structure shows good results – return loss below –10dB up to 85 GHz. It can be concluded that with the increase in the overlapping area (bump pad diameter) the return loss is increasing. It is recommended that the bump pad diameter should be kept to a minimum – decreasing the bump pad diameter and the bump diameter improves the performance of the transition. The bump pad size is a sensitive parameter – it is recommended to use bump pad dimensions as small as possible.

References

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