MODELING AND SIMULATION OF SHORT CIRCUIT CURRENT AND TRV TO DEVELOP A SYNTHETIC TEST SYSTEM FOR CIRCUIT BREAKERS

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Abstract: A parallel injection of short circuit current and transient voltage to medium and high voltage circuit breaker (CB) by a synthetic model is studied. Transient recovery voltage is created by a capacitor bank and is applied to CB. Also short circuit current is supplied by a 20/0.765 Kv short circuit transformer. Texas DSP is used as controller and programmed in code composer.
To test of circuit breakers by synthetic test equipments, an accurate control system can satisfy the test criterion. An optical triggered spark gap has been used to interrupt short circuit current and to initialize of transient recovery voltage (TRV) that is applied across the contacts of circuit breaker.
Modeled results are verified by a laboratory based synthetic test system. Test object CB is a 24 Kv, 25 KA with vacuum type chamber.
To find a desired sequence to open/close of backup- test object and auxiliary circuit breakers within appropriate time to inject of recovery voltage is main goal of the presented paper. Modeling and simulation has been done in MATLAB software. Test procedure has been done under IEC 62271-100, 62271-101.
Key words: Synthetic test, Medium voltage circuit breaker, Short circuit current, TRV.

I. Introduction

The circuit breaker used in the power network is close in the normal situation but it must be opened to protect network if there are abnormal event.
So in short-circuit occurrence, the circuit breaker will clear the high current by interruption and make re-closing duty to other sequences.

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IEC and ANSI/IEEE standards define circuit-breakers short-circuit tests (Isc) [1], [2]. IEEE_ C37 and IEC 62271 electrical standards manage the ratings, performance, features, and testing of circuit breakers.

At the test, short-circuit interrupting current with the full rated voltage is generally not possible in direct tests circuits where one source delivers the required current under the specified voltage.

Synthetic circuits where current and voltage are delivered by separate sources are designed to supply a short circuit current and recovery voltage. It is used for terminal fault interruption and are described in ANSI/IEEE guide C37-081 and IEC guide 427 [3], [4].

Single-phase tests can reveal the interruption of all three phases in a single operation and the method is applied for testing. Although to reproduce the real conditions of a three-phase interruption, it cannot be enough.

Standards oblige that interruption of 100% of Isc be prepared by a symmetrical current as T100s or TD4 and an asymmetrical current as T100a or TD5. Asymmetrical current is summation of an ac and a dc component declining with a time constant of 45 ms (X/R=58 at 50 Hz), dc component is over 20% [5]-[7].

The aim of this article is to present a test procedure for single-phase synthetic testing in a different scenario rather than other models.

Different researchers and organizations studied around the synthetic test. Denis Dufournet and Georges Montillet [8] claimed to present a procedure for three-phase synthetic testing which can properly test the circuit-breaker at a reasonable cost, i.e., a number of tests using a limited number of circuit-breaker specimen for the entire series of type tests. They deal around the theoretical calculations and they didn't suggest a practical laboratory test model.

Jung-Hyeon Ryu et. Al [9] studied on the symmetrical current to give the maximum prearcing energy and asymmetrical current to give the maximum electro-dynamic force. They expressed their circuit used minimum number of voltage circuit, measuring device for current and voltage, plasma making switch and auxiliary breaker. The lack of the job was that it had no special consideration for the test of dead tank GCB intended for GIS (gas insulated switchgear).

L. van der Sluis et al studied on the influence of the arc voltage in system test circuits [9]. different arc voltage waveforms and KEMA arc models are used to study the stress of the direct SLF (short line fault) test circuit and the synthetic SLF test circuit on the TB (test breaker). For the synthetic test circuit the total arc energy input in the TB is less than the direct test circuit, but just before the current zero the dI /dt and subsequently the arc energy input in the TB is higher. It is demonstrated that the arc-circuit interaction plays an important role for the TB to clear the fault. For SF6 breakers with an arc voltage with a significant extinguishing peak, the voltage injection synthetic test circuit produces an overstress for the TB. The authors studied on the different effects of energy at arcing time in direct and synthetic tests.

Author in the presented paper tried to introduce a model that can be competitive with direct test method, applied energy during short circuit to be high, test system to be low cost- reliable and low time.

II. Single-phase synthetic test procedure

According to figure 1, a synthetic test circuit has two different sources of current and voltage.

Before the test operation, arcing time, or period between contact separation and arc extinction at current zero, is defined. The arc is made by the high short circuit current source and at the chosen current zero time the recovery voltage is affected by the voltage source.

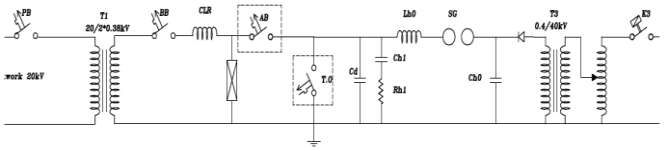

Figure 1. A synthetic test circuit presented by JDEVS.

An important message in the test is related to the implementation of recovery voltage over the arc. At the symmetrical current interruption (T100 or TD4), the characterization is slightly easy. As current zeros are showing every 60 electrical degree. The imposing time for recovery voltage has been defined by IEC standard. It is in final quarter of last half cycle. SABER software is usually used to simulate of short-circuit

III. Circuit equipments technical specification

A. Test object CB spec.

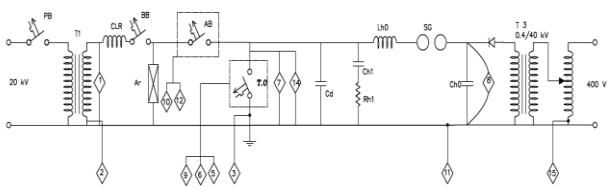

Figure 2. Sampling device position

Table 1. TO CB Spec.

Manufacturer	Parss Switch Co
Type	VD4 P
Nominal Voltage (kV)	24
Nominal Current (A)	2500
Frequency (Hz)	50
RMS Breaking Current (kA)	25
RMS Making Current (kA)	65
Operating Voltage (kV)	20
Operating sequence	O-0.3sec-CO-3min-CO
S.N	230453

B. CB contact separation timing determination

In no load condition timing process has been done, see table 3-4. When current is flowing in test object (TO) CB contacts, DSP controller send an open signal to CB trip coil and the interruption time is distinguished and measured. The time interval between trip signal sending and interruption time declared and calculated as contacts separation time.

Table 2. Contact separation (ms) for TO CB

Item	Contact Separation (ms)	Opening Coil Voltage (V)
1	44.155	125
2	43.950	125
3	44.110	125
Average	44.070	125

Table 3. Contact separation (ms) for AB CB

Item	Contact Separation (ms)	Opening Coil Voltage (V)
1	46.410	125
2	46.700	125
3	46.450	125
Average	46.520	125

IV. Simulation

To more investigation and to ensure of calculations in voltage and current of synthetic unit, different simulation has been done. MATLAB, ETAP, CYME,etc is used to modeling and simulation of process. Due to large wide domain of simulations, the following items listed and simulated.

- Simulation for T10, T30, T60 and T100 in order to calculation of parameters cited in IEC 62271 and IEC 62271-101 with a reasonable tolerance.
- Different arcing models simulation.
- Arc combined models Mayer+Casie simulation.
- Simulation of arc voltage effect on the half last cycle of current in vacuum and SF6 CB.
- Close direct asymmetrical (Cdasym) test simulation and synchronous CB fire angle assessment for asymmetrical current.
- Symmetrical (Cssym) test simulation and synchronous CB fire angle assessment for symmetrical current.
- Simulation for T10, T30, T60 and T100 interruption test.
- Simulation to define CLR to perform T10, T30, T60, T100 and closing tests.
- DC components determination simulation (with respect to switching time)
- Charging circuits of capacitors C_{h0} simulation with respect to charge time, charge current and other parameters.
- R_{h1} Resistance simulation with respect to voltage and discharged energy.
- Simulation and evaluation of current and voltage on the all of elements.
- Resistance of L_{h1} reactance simulation with considering to voltage drop regulation.
- 20Kv feeder simulation to choose a proper feeding transformer.
- Short circuit level and X/R of network simulation.
- The effect of number of network parallel transformer simulation.
- The effect of laboratory distance with feeding substation on the test by simulation.
- Effect of short circuit current power of current injection transformer and X/R ratio on the test by simulation.
- Simulation of surge arrester performance when malfunction operation in AB occurs.
- Simulation of test unit and network in order to set of relays and fuses.

A. Transient recovery voltage simulation:

Simulation performed for a 36 Kv, 31.5 KA CB in T100 test. The results for injected current by synthetic circuit and TRV voltage are shown in the figures 3.

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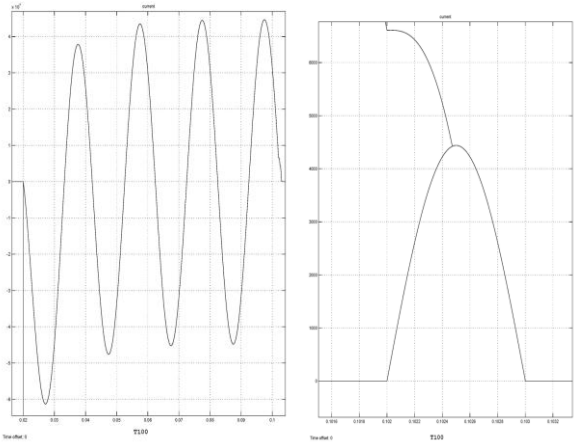

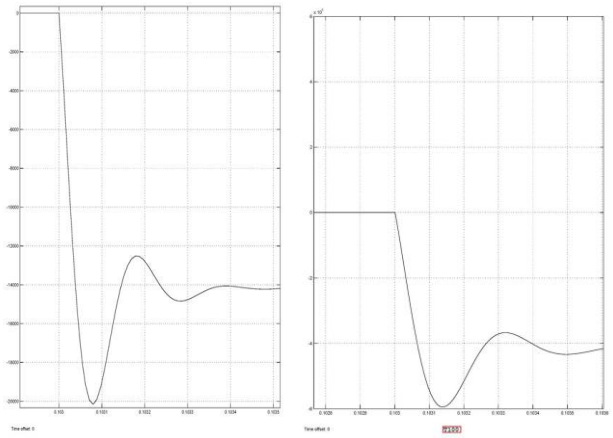

Figure 3. TRV trace by simulation T100 (100% current) results

B. Results and discussion for simulation application

Parameters such as Uc, t_3, td, dU/dt resulted by simulation are shown in table 4, Fig 17. The numen cultures are found in IEC 62271 and are according with IEC 62271-100, 4.102. Table 5 shows the parameters in IEC 62271-100. Table 6 shows a method to regulate of parameters to reach the ranges.

Table 4. Simulation results of parameters according to IEC 62271-100.

Ur kV	Ir kA	Test duty	Uc kV	t3 µs	td µs	dU/dt kV/µs	U_{h0} kV	C_{h0} µF	L_{h1} mH	R_{h1} Ω	C_{h1} µF	C_{hd} nF
36	31.5	T100	62.3	106.1	15.9	0.59	42.7	32.2	3.15	41	0.857	95.2
36	18.9	T60	66.4	44	6.6	1.51	45	19.3	5.25	171	0.089	9.9
36	9.45	T30	66.1	22.6	3.4	2.93	43.5	9.6	10.5	684	0.012	1.3
36	3.15	T10	66.3	21.4	3.2	3.09	38.5	3.2	31.5	2052	0.003	0.4
24	31.5	T100	41.3	86.4	13	0.48	28.3	48.2	2.1	34	0.832	2.6
24	18.9	T60	44.2	38.7	5.8	1.14	30.5	28.9	3.5	138	0.095	10.6
24	9.45	T30	45.3	19.5	2.9	2.33	30.4	14.5	7	552	0.01	1.1
24	3.15	T10	44.1	16.9	2.5	2.6	26.1	4.8	21	1656	0.003	0.4

Table 5. Parameters values in the IEC62271- 100

Urated kV	Irated kA	Test duty	Uc kV	t3 µs	td µs	dU/dt kV/µs
24	31.5	T100	41	87	13.1	0.47
24	18.9	T60	44	38	5.7	1.16
24	9.45	T30	44	19	2.9	2.32
24	3.15	T10	44	19	2.9	2.32
36	31.5	T100	62	109	16.4	0.57
36	18.9	T60	66	46	6.9	1.43
36	9.45	T30	66	23	3.5	2.87
36	3.15	T10	66	23	3.5	2.87

Table 6. Effect of each element on parameter such as: dU/dt, TRV, t3.

dU/dt		TRV	T3	
Low sensitive	-	+	+	C_{h0}
Low sensitive	-	+	+	L_{h1} ↑
High sensitive	--	-		C_{h1} ↑
	Fix	-	-	R_{h1} ↑
Very low sensitive	+	+	+	C_d ↑↑↑

With considering to the results, the best way to achieve an allowed range of tolerance for t_d , TRV , du/dt are to change capacitance of ch1 and charge voltage of C_{h0}. Other elements rest doesn't change. See table 6.

V. Test

A. Test procedure

- Timing calculation for TO and AB and so spark gap when the current is in a same polarity with current injected by voltage circuit.
- Few cycle delay to eliminate of asymmetrical current
- Zero crossing detection
- Closing pulse to TO and AB according to zero crossing
- Trigger pulse imposing on SG in ±30-50µs
- Closing pulse to BB CB after 200 ms.

The full test procedure is accessable in IEEE C37.013.

B. T60 (60% current) synthetic test

Table 5 shows that the parameters extracted by simulated results have a good fitness with IEC 62271-100, table 8. The values are used to the main model and results are shown in the figures 4.

Table 7. Values of elements for T60 test.

	Ur kV	Test duty	Uh0 kV	Ch0 µF	Lh0 mH	Rh1 Ω	Ch1 µF	Cd nF	CLR µH	Current source voltage
Calculated Values	**24**	**T60**	**31.4**	**23**	**4.41**	**174**	**0.076**	**8.4**	**60**	**760**
Test (1)	24	T60	30.5	23	4.4	192	0.071	8	60	760
Test (2)	---	---	---	---	---	---	---	---	---	
Test (3)	---	---	---	---	---	---	---	---	---	

Table 8. Results for parameters in T60

Item	Ur kV	Ir kA	Test duty	Isym kArms ±10%	IL²k A(rms) <-10%	TRV kV +10 %	t_3 µs	td µs ±20 %	dU/dt kV/µs +15%	Description	Test Result
IEC 62271-100	24	25	T60	15		44	38	6	1.16		
Test (1)	24	25	T60	15.6	<10 %	47.4	40	6.3	1.18	*	passed

Item	Ur kV	Ir kA	Test duty	Isym kA +5%	Current final loop <-10%	TRV kV +10%	t_3 µs	td µs ±20%	dU/dt kV/µs +15%	Description	Test Result
IEC 62271	24	25	T100	25		41	87	13.1	0.47		
Test (1)	24	25	T100	24.7	<-10%	49.2	---	---	---	*	Need tuning
Test (2)	24	25	T100	24.7	<-10%	39	---	---	---	**	Need tuning
Test (3)	24	25	T100	24.7	<-10%	39	---	---	---	***	Need tuning
Test (4)	24	25	T100	24.7	<-10%	49.2	---	---	---	****	Not passed

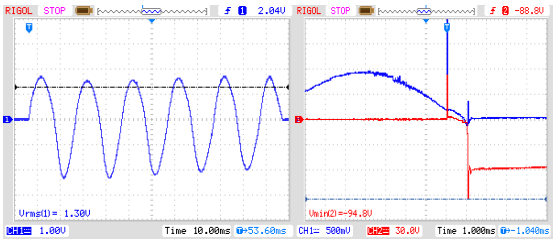

Fig 4. TRV Voltage and current in TO CB at the last half cycle with sampler no 14 with turn ratio of 500 Fig 6. Current through TO CB, sampling by CT 6000/1.

Short circuit current imposed to the TO CB in 6 cycles. It has a large duration and can damage to the network, in repetitive tests. TRV voltage shows a good trace but current shows a disturbance in the end of cycle. It may relate to the sampling sensors. Totally figures show a successive test for T60.

C. T100 test

The simulation results led to parameters determination. Using the parameters, test performed and the results clustered in the tables 9-10.

Table 9. Values of elements for T100 test.

	Ur kV	Test duty	Uh 0 kV	Ch 0 µF	Lh 0 mH	Rh 1 Ω	Ch1 µF	Cd nF	CLR µH	Current source voltage V
Calculated Values	24	T100	29.4	38.3	2.65	42	0.661	73.4	15	760
Test (1)	24	T100	29	38.3	2.6	42	0.638	68	20	760
Test (2)	24	T100	29	38.3	2.6	42	0.638	68	20	760
Test (3)	24	T100	29	38.3	2.6	42	0.638	68	20	760
Test (4)	24	T100	29	38.3	2.6	42	0.638	68	20	760

Table 10. Results for parameters in T100

*. AB_Open_time = 46520, SG_Delay_trig_time = 1300,, Dealay_AB_relative_TO=2000, TO_Open_time = 44072

**. Dealay_AB_relative_TO=2000, TO_Open_time = 44072, AB_Open_time = 46520, SG_Delay_trig_time = 2000

***. Dealay_AB_relative_TO=500, TO_Open_time = 44072, AB_Open_time = 46520, SG_Delay_trig_time = 2000

****. Dealay_AB_relative_TO= -500, TO_Open_time = 44072, AB_Open_time = 46520, SG_Delay_trig_time = 2000

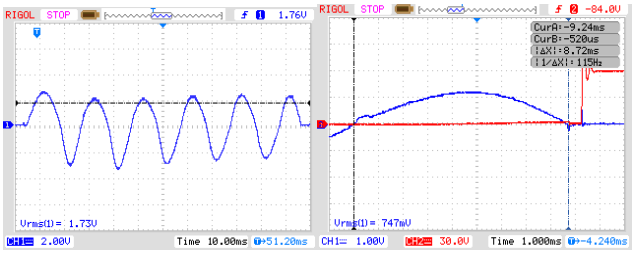

Fig 5. Test 1:TRV Voltage and current in TO CB at the last half cycle Fig 6. Current through TO CB, sampling

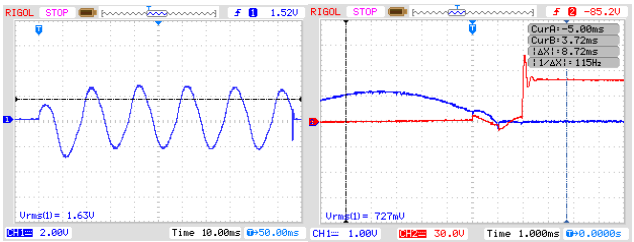

Fig 7. Test 2:TRV Voltage and current in TO CB at the last half cycle Fig 8. Current through TO CB, sampling

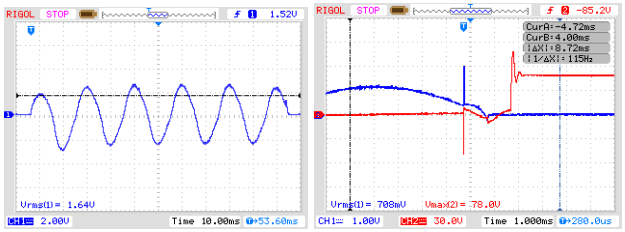

Fig 9. Test 3:TRV Voltage and current in TO CB at the last half cycle Fig 10. Current through TO CB, sampling

[2] **Current final loop**

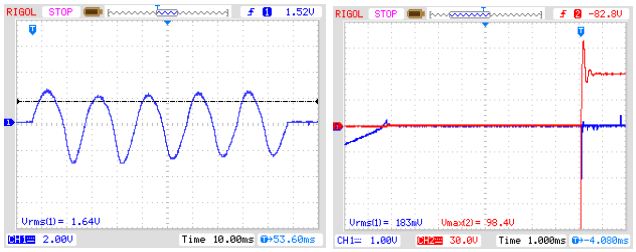

Fig 11. Test 4:TRV Voltage and current in TO CB at the last half cycle Fig 12. Current through TO CB, sampling

Figures 5-6 for test no 1 show that last half cycle duration decrease from 10 ms to 8.72. Then TRV voltage applied to TO in about 700 ms later. For this reason, delay time for trigger surge gap tuned and test repeated. The results of second test showed in figures 7 and 8. According to the figure, with voltage injection in a correct time, TRV voltage appeared after a full cycle current with 500 Hz. The phenomena can be resulted by a restrike in AB CB that causes to flow current by voltage circuit to AB CB.

Test 3 shows in figures 9-10. Delay time to open AB CB decrease from 2000 µs to 500µs. it can help to make a better condition for AB and TO CB. Because arc time and contacts distances are increased rather than to test 2. Also, restrike in AB can be expected to be cleared.

But achieved results that showed in figures 11-12 demonstrate again a restrike in AB CB. It means AB CB cannot tolerate source TRV voltage.

Delay for opening time of AB CB retuned where AB open sooner than TO CB in Test 4. In this case, AB CB opened sooner than TO with 500 µs. Meanwhile, figures 11-12 show that AB opened again sooner and it is not correct.

Then T100 can be successive if AB CB changes by a 31.5 KA ones. It can resolve restrike problem and can allow the first To be opened and then AB remove the main network connection with test circuit.

A test with more DC component performed and results show in figures 13-14. It seems DC components is more than 20% and the current cab be assumed an asymmetrical current. The change in current have no a significant difference by symmetrical current in the last quarter of current in the final cycle.

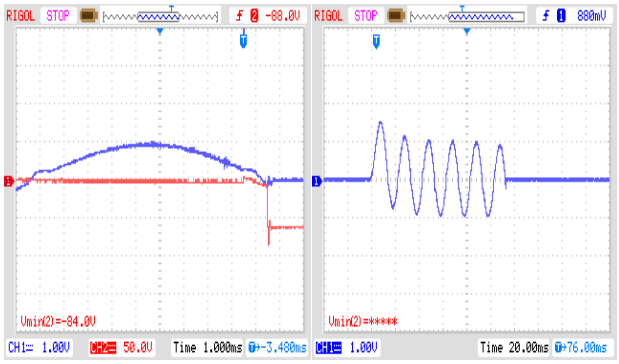

Fig 13. Test 5:TRV Voltage and current in TO CB at the last half cycle Fig 14. Current through TO CB, sampling

VI. Conclusion

A synthetic test rearranged and test performed. Results show the voltage and current circuit are correct. The main problem to test by short circuit transformer is related to network. Most of electricity utilities don't allow to test by this type transformer, because of that the repetitive high currents damages to network and can be led to operate of over current relays.

In other hand AB circuit breaker have to be one grade higher than TO. It means to test a 25 KA CB, AB must be 31.5 KA. It may can solve the problem by restrike.

In the presented paper, authors simulated the model and parameters extracted by simulation. The simulated results had a good convergence by IEC values. Also, test has been done by the resulted simulation parameters.

VII. References

[1] , IEC Standard 56 or 60056 (1987).
[2] , ANSI/IEEE Standard C37-09 (1979).
[3] Guide for Synthetic Fault Testing of AC High-Voltage Circuit-Breakers Rated on a Symmetrical Current Basis, ANSI/IEEE C37-081. [4] , IEC Standard 427 (1989-10).
[5] , IEC Technical Report 1633 (1995).
[6] Supplement to IEEE Guide for Synthetic Fault Testing of AC High-Voltage Circuit-Breakers Rated on a Symmetrical Current Basis, IEEE Standard C37-08la-1997.

[7] High voltage circuit breaker standards—comparative guide, Stephen M. Cary, May 2013, www.eaton.com/
[8] Denis Dufournet et al, Three-Phase Short Circuit Testing of High-Voltage Circuit Breakers Using Synthetic Circuits, IEEE transaction on power delivery, VOL. 15, NO. 1, JANUARY 2000, pp 142/148
[9] Jung-Hyeon Ryu, Ike-Sun Choi and Kern-Joong Kim, Three-phase Making Test Method for Common Type Circuit Breaker, Journal of Electrical Engineering & Technology Vol. 7, No. 5, pp. 778~783, 2012, http://dx.doi.org/10.5370/JEET.2012.7.5.
[10] L. van der Sluis and B.L. Sheng, the influence of the arc voltage in synthetic test circuit, IEEE Transactions on Power Delivery, Vol. 10, No. 1, January 1995. Pp 214-220.

VIII. Acknowledgements

The author is pleasure to express thanks to Tavanir to finance the project and JDEVS-Tehran, to test facility.

IX. Appendices

The following tables 11-14 and figure 15 show the equipment specifications.

Table 11. Current circuit spec.

No.	Detail	Equipment
1	S_n = 3.15 MVA U_{1n} = 20 kV U_{2n}= 2 * 380 V Uk% = 6 X/R > 10	Short Circuit Transformer (T1)
	U_{rated} = 850 V	Surge arrester to protect of Tr.
4	L =60µH U_n = 1 kV I_{SC} = 31.5 kA	Limiting current reactor LV (CLR)
1	V_n = 24 kV I_n =2500 A I_{sc}=25 kA Type: VD4 S.N: **230453**	(AB) Auxiliary vacuum CB (Auxiliary Breaker)
1	V_n = 24 kV I_n =2500 A I_{sc}=25 kA Type: VD4 S.N: **250321**	Vacuum CB (BB) (Back Up Breaker)
1	V_n = 24 kV I_n =2500 A I_{sc}=25 kA Type: VP4 S.N: **250238**	Vacuum CB (TO) (Test Object)

Table 12. Voltage circuit spec.

No.	Detail	Equipment	Row
93	4000nF	Main capacitor (Ch_0) 12kVAC± 10%	1
3	2000nF		
3	1000nF		
3	500nF		
3	250nF		
3	125nF		
1	40kV/30kVA	High voltage source(T_3)	٢
1	140 kV_DC	High voltage diode with resitance	3
1	400V /100 kVA	Auto transformer	٤
3	20 taps from: 0.65 ~ 25 (mH)	Reactor (Lh_1)	5
2	One 6 taps and one 5 taps capacitor	Capacitor (Ch1)	6
14	Resistances: 0.5 – 4096 Ω	Resitance (Rh1)	7
2	One 6 taps and one 5 taps capacitor	Capacitor (Ch_d)	8
1	In 3 range of voltage	Surge Gap (SG)	9
1	With delay: ±10 µs	Trigger Unit	10
33	20 kVDC	Pneumatic CB 20 kV	11
3	60 kVDC	Pneumatic CB 60 kV	12
---	Vinyl epoxy and ST 38	Structure	13

Table 13. Control and monitoring equipment spec.

No.	Detail	Equipment
1	Texas Instruments DSP TMS320F2812, 150 MHz 16 ADC, 12 bit, 2 M/s Digital Input: 8 Digital Output:8 Output Relay :16	Microcontroller
1	Analogue Input:16 Analogue Output:16	Signal conditioning board
1	GUI MATLAB	Software
1	Fully shilded	Industrial Case
1	Intel	Computer
1	34 Unit Mazdak type	Control Panel
2	2 Channel, 60 MHz RIGOL	Oscilloscope

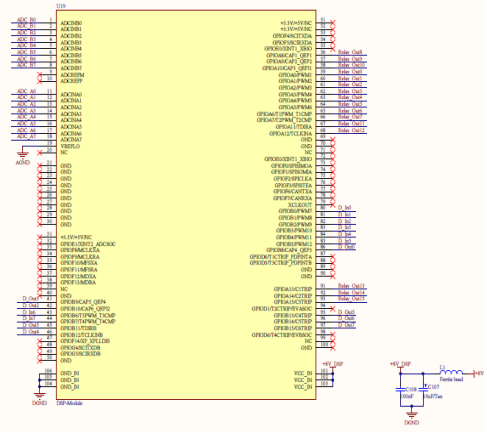

Figure 15. DSP model

Table 14. Sampling devices spec

Ratio	Attenuation ration for conditioning signal board	Attenuation ration for sampler	Sampling Spec.	Description	Signal No.
1200	1200	1	760V	Secondary voltage of T1	1
50000	2	25000	1500 A / 60 mV/ 40μΩ	Secondary current of T1	2
10000	2	5000	300 A / 60 mV / 200 μΩ	TO Current	3
50000	2	25000	1500 A / 60 mV/ 40μΩ		
12000	----	12000	CT 6000/1 / 5 VA & Burden=0.5 Ω		
2	2	-----	Current Shunt resistance 0.5Ω	Opening coil of TO	5
2	2	-----	Current Shunt resistance 0.5Ω	Closing coil of TO	6
120	2	60	2 MΩ	TO voltage (Arc voltage)	7
56000	200	280	280 MΩ	Ch_0 voltage	8
2	2	-----	0-5V Inductive sensor	Traveling TO	9
2	2	-----	Current Shunt resistance 0.5Ω	Closing AB	10
2500	2	1250	75 A / 60 mV / 800 μΩ	Synthetic current	11
2	2	-----	Current Shunt resistance 0.5Ω	Opening coil of AB	12
60000	120	500	100 pF,100kV	TO voltage (TRV)	14
333	2	166.7	10 A / 60 mV / 0.6 mΩ	Primery current of T3	15

Figure. 16. Test set up

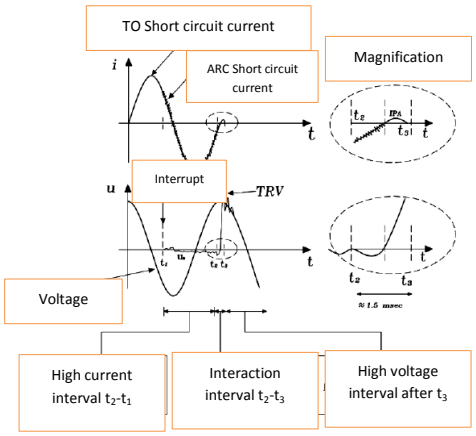

Figure. 17. Interruption sequences.